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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/501,287	01/18/2005	Maria Del Rocio Martin Lopez	10191/3702	5683

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KENYON & KENYON LLP
ONE BROADWAY
NEW YORK, NY 10004

EXAMINER	
CHIU, TSZ K	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/501,287	LOPEZ ET AL.	
	Examiner	Art Unit	
	Tsz K. Chiu	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-14 and 18* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

Claim 16 is objected recites the limitation "the coating" in page 5 line 7. There is insufficient antecedent basis for this limitation in the claim. The examiner suggest that claim 16 should be depend from claim "15".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

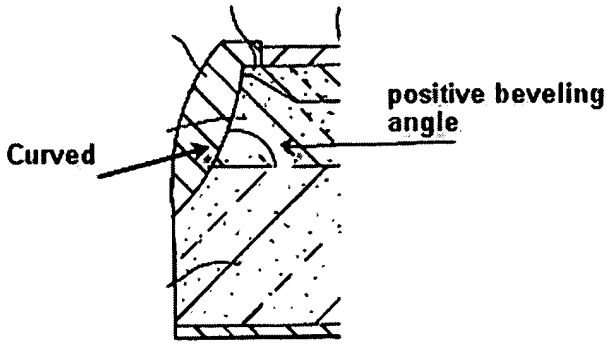
> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Davis (5,930,660).

With respect to claim 9, Davis discloses a PN transition (14, For example Fig. 4); and a chip having an edge region (18b, For example Fig. 4), the chip including a first layer (12, For example Fig. 4) of a first conductivity type and a second layer (10, For example Fig. 4) of a second conductivity type opposite to that of the first conductivity type, the first layer having the edge region (18b, For example Fig. 4) and a center region (18a, For example Fig. 4), the PN transition (14, For example Fig. 4) being provided between the first layer (12, For example Fig. 4) and the second layer (10, For example Fig. 4); wherein the second layer is more weakly doped in the edge region than in the center region (column 2, lines 29-37), and the boundary surface (14, For example Fig. 4) of the pn transition is non-parallel to the main chip plane at the edge region (edge of 10, For example Fig. 4).

With respect to claim 10, Davis discloses the pn transition includes a diode (column 1, lines 19-21).

With respect to claim 11, Davis discloses the boundary surface of the pn transition includes a positive beveling angle at the edge region (see drawing below).



With respect to claim 12, Davis discloses the boundary surface of the pn transition is curved at the edge region (see drawing above in claim 11).

With respect to claim 13, Davis discloses a thickness of the chip is less at the edge region (18b, For example Fig. 4) than in the center region (18a, For example Fig. 4).

With respect to claim 14, Davis discloses forming a pn transition (14, For example Fig. 1); forming a chip having an edge region (18b, For example Fig. 3), the chip including a first layer (12, For example Fig. 1) of a first conductivity type and a second layer (10, For example Fig. 1) of a second conductivity type opposite to that of the first conductivity type, the first layer having the edge region (18b, For example Fig. 3) and a center region (18a For example Fig. 3), the pn transition (14, For example Fig. 3) being provided between the first layer (12, For example Fig. 4) and the second layer (10, For example Fig. 4); and doping the second layer more weakly in the edge region

than in the center region (column 2, lines 29-37), wherein a boundary surface (14, For example Fig. 4) of the pn transition is non-parallel to the main chip plane at the edge region (edge of 10, For example Fig. 4); and wherein the first layer is manufactured using patterned doping (column 3, lines 44-53).

With respect to claim 18, Davis discloses the chip is pre-coated with dopant via at least one of APCVD deposition of a doped glass, a doping film, a gas phase coating, ion implantation, and an application of doping pastes (column 2 lines 49-50).

Allowable Subject Matter

Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance: The prior art made of record and not relied upon in considered pertinent to applicant's disclosure. Davis (5,930,660) and Schoenberg (5,150,176) relate to pn junction diode; Davis discloses forming a pn transition and forming a chip having an edge region, the chip including a first layer of a first conductivity type and a second layer of a second conductivity type opposite to that of the first conductivity type, the first layer having the edge region and a center region, the pn transition being provided between the first layer and the second layer; and doping the second layer more weakly in the edge region than in the center region, wherein a boundary surface of the pn transition is non-parallel to the main chip plane at the edge region; and wherein the first layer is manufactured using patterned doping, but fail to teaches the patterned doping is provided by pre-

coating the chip with dopant, subsequently removing the coating in a sub-region of the chip, and subsequently introducing the dopant into the chip.

Therefore, claim 15 is presently allowed.

Claim 16 would be allowable if rewritten to overcome the objection, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Furthermore claim 17 would be allowable if claim 16 is rewritten to overcome the objection, for the reason that claim 17 is dependent on claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tsz K. Chiu whose telephone number is 517-272-8656. The examiner can normally be reached on 0800 to 1700.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TKC
January 4, 2006

ZANDRA V. SMITH
SUPERVISORY PATENT EXAMINER
8 January 2006